Amendments to the Claims

The Claim Listing below replaces all prior versions of the claims in the subject application.

Claim Listing:

Claim 1 (currently amended): A method, comprising:

receiving a plurality of packets with audio information sent using a first timing signal; and

reproducing said audio information using a second timing signal and compensating for time differences between said first and second timing signals using a circular buffer with a variable read out location, said circular buffer being to store said packets in buffer locations in said circular buffer corresponding to frequencies of network delays.

Claim 2 (cancelled).

Claim 3 (currently amended): The method of claim 1 2, further comprising building a histogram to represent a probability distribution for a given set of network delays, said histogram having a plurality of levels with each level representing a respective

frequency of network delay, and with each level corresponding to a respective buffer location in ~~for~~ said circular buffer.

Claim 4 (original): The method of claim 3, wherein said reproducing comprises:

determining a first delay value for each packet;

storing each packet in a buffer location using said first delay value;

updating said histogram using said first delay value;

determining a read out location for said circular buffer; and

reading each packet from said buffer using said read out location.

Claim 5 (original): The method of claim 4, wherein said storing comprises:

determining a second delay value for each packet; and

storing each packet in a buffer location corresponding to said second delay value.

Claim 6 (original): The method of claim 5, wherein said determining said second delay value comprises:

retrieving a third delay value;

comparing said first delay value with said third delay value; and

determining said second delay value in accordance with said comparison.

Claim 7 (original): The method of claim 6, wherein said first delay value represents a network delay, said second delay value represents a packet delay value, and said third delay value represents an optimal delay value.

Claim 8 (original): The method of claim 4, wherein said updating said histogram comprises:

estimating a time difference between said first and second timing signals; comparing said time difference to a threshold parameter; and

updating said histogram in accordance with said comparison.

Claim 9 (original): The method of claim 8, wherein said estimating said time difference comprises:

determining an average packet delay value for said plurality of packets using said histogram on a periodic basis;

analyzing said average delays for a linear change; and

estimating said time difference based on said linear change.

Claim 10 (original): The method of claim 9, wherein said time difference is greater than said threshold parameter, and updating said histogram in accordance with said comparison comprises assigning each level a new buffer location within said circular buffer.

Claim 11 (original): The method of claim 10, wherein said circular buffer includes a jitter buffer comprising a subset of said buffer locations, with said jitter buffer having a start buffer location and an end buffer location, and said histogram has a start level and an end level, and said assigning comprises:

assigning said end level corresponding to said end buffer location to a next buffer location of said circular buffer; and

shifting said remaining levels by one buffer location towards said end buffer location.

Claim 12 (original): The method of claim 11, wherein determining said read out location comprises determining a buffer location corresponding to said end level.

Claim 13 (currently amended): A system, comprising:

a first wireless transceiver;

an omnidirectional antenna to couple to said first wireless transceiver; and

a jitter buffer module (JBM) connected to said first wireless transceiver, said JBM further comprising a Clock Compensation Module (CCM), said JBM also comprising a circular buffer with a variable read out location, said circular buffer being to store packets in buffer locations in said circular buffer corresponding to frequencies of network delays.

Claim 14 (original): The system of claim 13, wherein said system further comprises:

an encoder connected to said first wireless transceiver; and

a first timing device connected to said encoder and said first wireless transceiver.

Claim 15 (original): The system of claim 14, further comprising:

a second wireless transceiver;

an omnidirectional antenna to couple to said second wireless transceiver;

a JBM connected to said second wireless transceiver, said JBM having a CCM; and

wherein said second wireless transceiver further comprises a decoder connected to said second wireless transceiver, and a second timing device connected to said decoder and said second wireless transceiver.

Claim 16 (currently amended): The system of claim 15, wherein said JBM further comprises:

~~a circular buffer; and~~

a Buffer Management Module (BMM) connected to said circular buffer.

Claim 17 (currently amended): The system of claim 16, wherein said CCM estimates a clock differential value between said first and second timing devices using an average packet delay value from a histogram representing a distributional curve of said frequencies of network delays, and sends said clock differential value to said BMM.

Claim 18 (original): The system of claim 17, wherein said BMM receives said clock differential value from said CCM, and delays each packet a set amount of time using said clock differential value.

Claim 19 (currently amended): The system of claim 18, wherein in said circular buffer ~~comprises a plurality of buffer locations to store audio information, with~~ a subset of said buffer locations each corresponds ~~corresponding~~ to a level from said histogram.

Claim 20 (original): The system of claim 19, wherein said BMM delays each packet by selecting a buffer location to store each packet.

Claim 21 (original): The system of claim 20, wherein said BMM modifies which buffer location correspond to which level in accordance with said clock differential value.

Claim 22 (currently amended): An apparatus, comprising:

a receiver; and

a Jitter Buffer Module (JBM) connected to said receiver, said JBM further comprising a Clock Compensation Module (CCM) and a circular buffer with a variable read out location, said circular buffer being to store packets in buffer locations in said circular buffer corresponding to frequencies of network delays.

Claim 23 (currently amended): The apparatus of claim 22, wherein said JBM further comprises:

~~a circular buffer; and~~

a Buffer Management Module (BMM) connected to said circular buffer.

Claim 24 (currently amended): The apparatus of claim 23, wherein said CCM estimates a clock differential value between a first and second timing devices using an average packet delay value from a histogram representing a distributional curve of said frequencies of network delays, and sends said clock differential value to said BMM.

Claim 25 (original): The apparatus of claim 24, wherein said BMM receives said clock differential value from said CCM, and delays each packet a set amount of time using said clock differential value.

Claim 26 (original): The apparatus of claim 25, wherein said circular buffer comprises a plurality of buffer locations to store audio information, with a subset of said buffer locations each corresponding to a level from said histogram.

Claim 27 (original): The apparatus of claim 26, wherein said BMM delays each packet by selecting a buffer location to store each packet.

Claim 28 (original): The apparatus of claim 27, wherein said BMM modifies which buffer location correspond to which level in accordance with said clock differential

value.

Claim 29 (currently amended): An article comprising:

a storage medium;

said storage medium including stored instructions that, when executed by a processor, result in receiving a plurality of packets with audio information sent using a first timing signal, and reproducing said audio information using a second timing signal and compensating for time differences between said first and second timing signals using a circular buffer with a variable read out location, said circular buffer being to store said packets in buffer locations in said circular buffer corresponding to frequencies of network delays.

Claim 30 (currently amended): The article of claim 29, wherein the stored instructions, when executed by a processor, further result in performing said reproducing by determining a first delay value for each packet, storing each packet in a respective buffer location using said first delay value, updating said histogram using said first delay value, determining a read out location for said circular buffer, and reading each packet from said buffer using said read out location.